Design Fault Tolerant Full Adder Using Fault Localization

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***Abstract*— Many reasons lead to errors in digital circuits. some of these errors are often transient (including electromagnetic fields, cosmic radiation, and noise) and others permanent (a result of poor manufacturing, and storage). in two cases they leave a negative impact on the operation of these circuits. The size of these circuits is too small compared with their function and accuracy. these circuits are very sensitive to such errors, whether they are transient or permanent. The impact of transient errors on these circuits can be catastrophic in high-performance computing systems, where multiple processing units are used. Due to the importance of the Full Adder as a basic structure in building processors, a small-size fault-tolerant Full Adder is proposed in this paper. The proposed Full Adder possesses a high ability to detect and repair errors. The proposed design has a high reliability during work in real-time compared with previous designs.**

I. Introduction

Fault-tolerant systems are very sensitive, and that is difficult for humans to Interfering with them during work. The effectiveness of these systems appears in medical monitoring, safety systems, and space technology. the error in such systems will lead to undesirable results and may be disastrous in some cases. the technology imposes a set of rules in the designing process, such as reducing the size of the chip. As the chip gets smaller, it becomes more affected by electromagnetic fields and cosmic rays, which increases the chance of a malfunction or breakdown of these systems.

Full Adder is an important component in microprocessors and digital signal processors, it is the basic structure of arithmetic logic unit ALU. it is used in complex operations such as multiplication, division, and calculating address values. it is clear the bad effect of Full Adder on the processor if it gets an error [1][2].

The number of transistors in the design is very important to minimize the chip's size. so, researchers seek to provide designs that verify the requirement at the lowest cost and space. Gate-Diffusion-Input (GDI) is derived from CMOS technology. GDI provides a new control method in transistor operation, its main goal is to reduce the number of transistors on a chip and reduce the power consumed in the circuit [3-5].

The research proposes a self-correction Full Adder using CMOS and GDI technology. The proposed design reduces the space used in the chip. the proposed design tested in a 4-bit multiplier.

The main contributions of the paper are listed as follows:

• design a fault-tolerant Full Adder used in processors for medical monitoring systems and space systems.

• The proposed design detects and repairs errors, and has high reliability in detecting independent and non-independent single errors and double errors.

• The proposed design also provides the ability to detect synchronous and asynchronous double errors,

• The proposed design provides more space on the chip compared with others.

The rest of this paper is organized as follows. Section 2 illustrates a background and important related works. In section 3, the proposed design is presented. The simulation is illustrated in Section 4. The conclusion is presented in Section 5

II. Background and Related Works

The proposed design process depends on finding out the lack of previous models and proposing an appropriate solution. Therefore, the design stages can be described by the following steps:

- studying the concept of structural and temporal surplus.

- studying the concept of self-repair in fault-tolerant architectures.

- studying the concept of independent error detection.

- Study of design using CMOS and GDI technologies.

Time redundancy: In the time redundancy the system structure is doubled, and to protect it from error transmission a delayed clock pulse is used for the duplicated unit as shown in Figure (1). Then, the outputs of the two units are compared, and if the comparison results are identical, that means no errors. Vice versa, if the results are different that means an error exists. Researchers in [6] proposed a model of a Full Adder that detects errors using the concept of time redundancy. The main problem with this design is the time delay. where according to the computing process, the advance of signals is delayed before comparing the results. If the computing process contains an

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error, the error will spread throughout the entire system and the model cannot detect errors of type stuck-at.

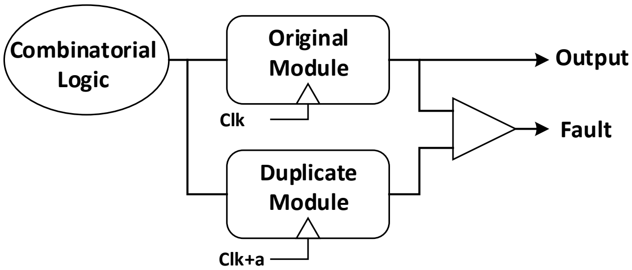

Figure 1. Time redundancy

Hardware redundancy: to achieve hardware redundancy, several modules are required in the design. The output of these modules is compared to detect the error. There are two commonly used types, the first is a model with a basic unit and an additional one (Double-modular redundancy (DMR)). the second model uses two additional modules and one basic module (Triple-modular redundancy (TMR)).

In DMR, the original functional unit is doubled. As shown in Figure (2.a), the two units are connected in parallel and their outputs are compared to check the errors. This model increases the system's reliability at a minimal cost [7], but it can detect a single error only without repair. the model doesn't fix the error because the multiplexer cannot determine its position [8].

In TMR, three copies of the original module are connected, as shown in Figure (2.b). The units are connected in parallel and their outputs are compared to check the errors. Errors in these units cannot be repaired if they are different and independent. However, the reliability of these systems is high [1]. The problem that this design suffers from is the space occupied by the chip, which increases by 300%. in addition to its inability to detect more than one error [9].

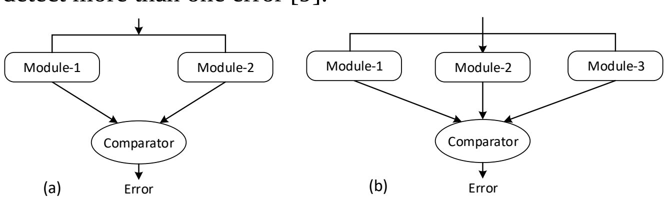

Figure 2. Double-modular redundancy (DMR), (b). Triple-modular redundancy (TMR)

A Full Adder with the concept of redundancy: The authors in [10] propose a model of self-repair Full Adder. The design can detect the error and repair it, which is an improvement model of the proposed one in [11]. The model consists of a Full Adder, two XNOR gates, a functional unit for error detection, and two Adders to repair the errors as shown in Figure (3). This design cannot detect double errors occurring simultaneously, because it depends on both signals the Carry (Cout) and the result (Sum) together. In addition, using independent functional units may increase the probability of an error occurring.

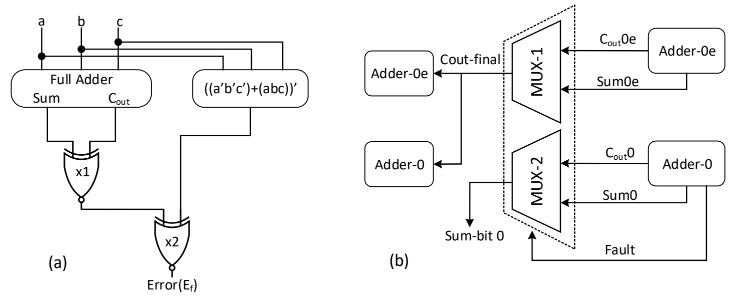

Figure 3. the proposed design in [10]

The researchers in [12] proposed an enhanced model of self-repair Full Adder. The design can detect independent synchronous and asynchronous errors. The model uses five XNOR gates and a functional unit. It also adopts the concept of redundancy to fix the errors. The model can detect errors and reduce the number of transistors on the chip compared to previous designs. the model depends on a functional unit (additional transistors) to detect the errors, which may occur during the computing process. So, the model doesn't provide a good enhancement in the number of transistors.

GDI technologies: In [13] the researchers present a model of a fault-tolerant Full Adder using double-pass transistor Logic (DPL) technology, that reduces the number of transistors on the chip but cannot detect double errors. The researchers in [14] present a model of a fault-tolerant Full Adder using the GDI design, that can detect double errors but the design does not provide good space.

III. PROPOSED DESIGN

The proposed design cancels the concept of the additional unit proposed in the model [10,12]. which increases the system's reliability, and enhancement the performance. The proposed model adopts the concept of independent error correction to solve the problem of synchronous errors. The proposed model shown in Figure (4).

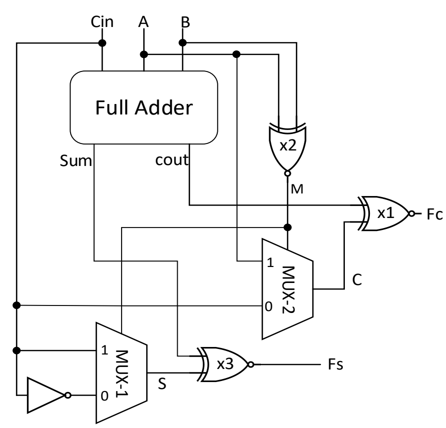

Figure 4. Proposed model for error detection

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A. Detecting errors in the proposed model

The proposed design detects the errors independently for both carry and sum. The proposed design in this paper eliminates the lack of the model in [10,12], it cancels the carry error-checking unit. And substitutes it with 3 XNOR gates and two multiplexers. The Carry Cout is compared with the C to obtain the signal Fc. Then, the Sum is also compared with S to obtain the control signal Fs. The logic equations of detection error as follows:

$Sum=(A\oplus B)\oplus C_{in}$ (1)

$C_{out}=A\,B+(A\oplus B)\,C_{in}$ (2)

$M=\overline{(A\oplus B)}$ (3)

$F_C=\overline{(C\oplus C_{out})}$ (4)

Signal M represents a pulse to the Multiplexers. If $F_C = 0$, the calculated carry matches the basic carry, and there is no error happen. and vice versa, if $F_C= 1$ there is an error in the value of the basic carry. The sum value is verified by the XNOR gate as the following relation:

$F_S=\overline{(S\oplus M)}$ (5)

If $F_S=1$ there are no errors in the calculated sum value, and vice versa if Fs=0 there is an error in the calculated sum. The previous equations and how the Full Adder detects the error are summarized in Table (1).

Table 1. Truth table for Full Adder with error detection

A	B	C_{in}	Sum	C_{out}	M	S	C	F_S	F_C
0	0	0	0	0	1	0	0	1	1
0	0	1	1	0	1	1	0	1	1
0	1	0	1	0	0	1	0	1	1
0	1	1	0	1	0	0	1	1	1
1	0	0	1	0	0	1	0	1	1
1	0	1	0	1	0	0	1	1	1
1	1	0	0	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1

B. Repaired method in the proposed model

The proposed model calculates the values of the control signals F_C and F_S, which express the presence or absence of an error. and the repairing is done by reversing the signals Fc and Fs using inverters as shown in Figure (5). The repairing is done by the following steps:

- The value of sum and carry is either 0 or 1 depending on the input values.
- The control signal F_S indicates the error in the sum value, so it is reversed by the multiplexer.
- The control signal F_C indicates the error in the carry value, so it is reversed by the multiplexer.

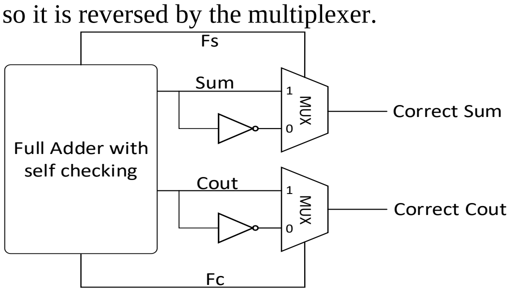

Figure 5. Repaired method in the proposed design

C. The chip size and the number of transistors

The proposed model reduces the number of transistors to 65 compared to previous designs, as shown in Table (2). The comparison is made using the following relationship, which expresses the excess space used in the chip.

$$Area_{overhead} = \frac{Area_{with\ FT} - Area_{Without\ FT}}{Area_{Without\ FT}} \times 100\% \quad (6)$$

Table 2. Comparison between designs in terms of the number of transistors and the chip size

design	Number of transistors in function unit	The total Number of transistors	CMOS Chip Size
Proposed design	1- Adder 28 3-XNOR 15 4-MUX 16 3-Inverter 6	65	132.14%
The design in [12]	1-Adder 28 2-XNOR 10 2-AND 14 1-OR 6 1-Fun unit 14 2-MUX 8 8-Inverter 16	96	242.85%
The design in [10]	2-Adder 56 4-XNOR 24 2- Fun unit 24 2-MUX 8	112	300%

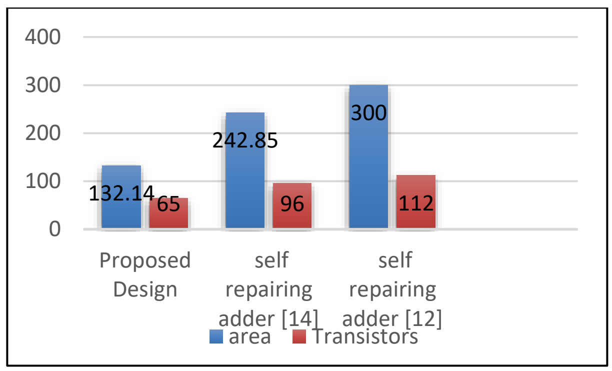

Figure 6. comparing the proposed design with the design in [12] and [10]

If we repeat the proposed design, but this time using logic gates based on GDI technology instead of CMOS [12][5][3]. We will obtain the results shown in Table (3)

Table 3. The proposed design using GDI

design	Number of transistors in function unit	The total Number of transistors
The design GDI	1- Adder 10 3-XNOR 12 4-MUX 8 3-Inverter 6	36
The design GDI in [12]	1-Adder 10 2-XNOR 8 2-AND 4 1-OR 2 1-Fun unit 14 2-MUX 4 8-Inverter 16	58

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D. Reliability

The system reliability calculated by the following relationship:

$$R_{SelfRepairing} = 1 - \frac{\binom{N-2}{r-2} \times n}{\binom{n}{r}} \quad (7)$$

Where n represents the number of Adder in one model, and N represents the number of Adder (FA) in a 4-bit multiplier. To test the reliability of the proposed design for synchronous and asynchronous double errors, we use it in a 4-bit multiplier (see figure (7)). the result is shown in Figure (8) and Table (4).

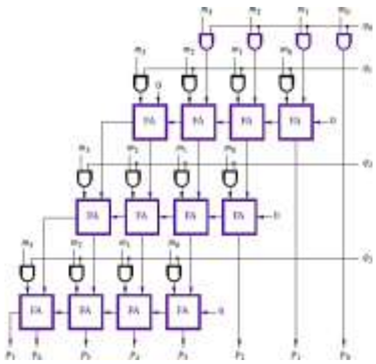

Figure 7. 4-bit multiplier

Table 4. Comparison of reliability results

	proposed design	The design in [10]	TMR
One error	100%	100%	100%
Double errors in 4-Bits Full Adder	100%	85.82%	27%

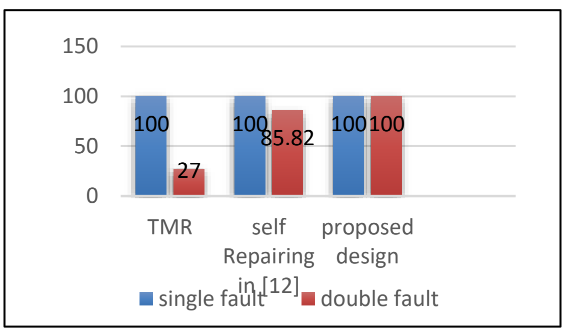

Figure 8. Comparison of reliability results

IV. SIMULATION

The simulation was done using the Microwind program. the error is inserted in the sum output and the carry. The results showed that the Adder corrects the errors in all cases whether it used CMOS or GDI technology, as shown in Figures (9-11).

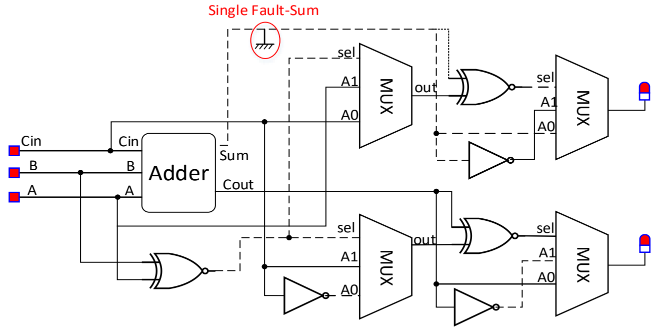

Figure 9. Single Sum error (using CMOS technology)

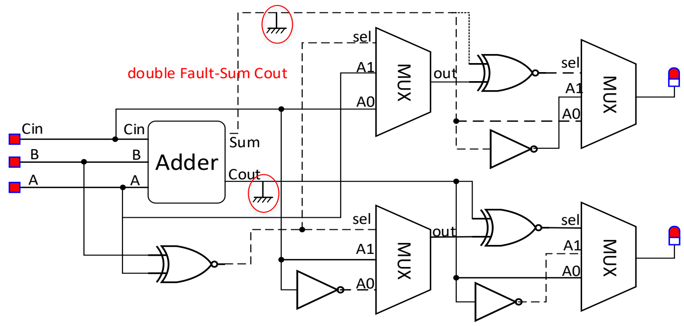

Figure 10. double Sum ,C_out error (using CMOS technology)

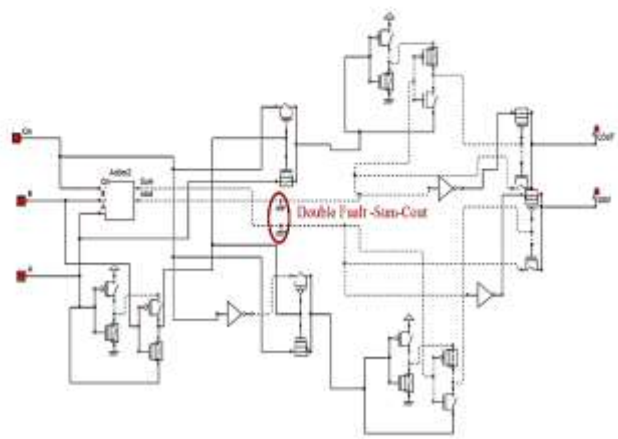

Figure 11. double Sum ,C_out error (using GDI technology)

V. CONCLUSIONS

The proposed design offers the following improvements:

- The proposed design is capable of detecting individual errors with 100% reliability.
- The reliability of the proposed design is 100% in detecting synchronous and asynchronous double errors.
- The number of the chip's transistors decreased to 65 transistors, and the volume they occupied as a logic result.
- The number of transistors in the fault-tolerant Full Adder using GDI technology is 36 transistors.
- Reducing the number of transistors reduces the overall cost of the design process.
- The total power consumed in the chip decreases as a result of the decrease in the number of transistors.

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The proposed design is very recommended in special systems like medical systems, safety systems, and space systems. Because error-free results in such systems are very important. In addition, the effect of the reduced number of Transistors is obvious in the processors that require a large number of Adders. which reduces the design cost and also reduces the size of the fault-tolerant chip.

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