Multiplierless low-cost implementation of Hindmarsh–Rose neuron model in case of large-scale realization

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Saeed Haghiri · Salah I. Yahya · Abbas Rezaei · Arash Ahmadi

Overview | Citations (3) | References (57)

Abstract

Implementation of neural networks in case of hardware helps us to understand the different parts of the human brain operation, using artificial intelligence (AI). This paper presents a new model of the Hindmarsh–Rose (HR) Neuron that is based on basic polynomial functions called Nyquist-look up table-Hindmarsh–Rose (N-LUT-HR) based on an accurate sampling of the original model. The proposed approach is investigated in terms of its digital realization feasibility. According to high matching between the original and proposed terms, it is showed that the new modified model can follow all spiking patterns of primary model with low-error computations. In hardware case, the proposed and original models are implemented on Xilinx FPGA XC2VP30 chip to validate different aspects of the simulation results. Hardware results demonstrate that our model regenerates the desired patterns in low-cost and high-frequency (speed-up) in comparison with the other similar works. Overall saving in FPGA resources show that this new model is capable of being used in large-scale networks in case of minimum required resources (FPGA costs). In addition, the analysis of hardware indicates that the new circuits can work in a maximum frequency of 123 MHz with 98.25% saving in FPGA costs (resources utilization of FPGA). In this paper, an FPGA realization of a new model of the Hindmarsh–Rose (HR) Neuron that is based on basic polynomial functions called Nyquist-look up table-Hindmarsh–Rose (N-LUT-HR) based on an accurate sampling of the original model is presented. This leads to achieve a high-speed multiplierless implementation. Results in MATLAB and Virtex-2 FPGA board demonstrate that our method can mimic the original model in high degree of similarity. Consequently, our reduced-model can be used in large-scale networks because of its low-cost hardware.