A new DVCC-based fully cascadable voltage-mode full-wave rectifier

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OUTLINE

- **Abstract**
- **Introduction & Literature Survey**
- **Comparison of the proposed rectifier with the previously published ones**
- **Circuit description**
- **Simulation results**
- **Conclusion**

Abstract

—A new VM full-wave rectifier circuit employing two DVCC+ , two grounded resistors, and two diodes is proposed.

—The proposed circuit enjoys high input impedance and low output impedance; accordingly, it is suitable for direct cascading with other VM circuits

—It employs only two grounded resistors which are advantageous for IC implementations.

—However, it needs a single resisitor matching condition.

—It is simulated using SPICE program to verify the theoretical analysis.

Introduction & Literature Survey

- Rectifiers are widely used in a number of areas such as wattmeters, AC voltmeters and ammeters, RF demodulators, signal-polarity detectors, averaging circuits, peak-value detectors, piecewise linear function generators, and various nonlinear analog signal-processing circuits.
- The operation of diode-only rectifiers is limited by the threshold voltages of diodes, approximately 0.3 V for germanium diodes and 0.7 V for silicon diodes.

Introduction & Literature Survey (Cont’d)

- Precision full-wave rectifiers using opamps were previously proposed.
- The action of the opamps effectively overcomes the threshold voltage of the rectifying diodes, which enables full-wave rectification of a low-level signal.

However, the full-wave rectifiers based on opamps and diodes while generally are faster than other rectifier circuits suffer from a major disadvantage.

Introduction & Literature Survey (Cont'd)

- The finite small-signal dV/dt of the opamps results in an important distortion of the rectified signal during the zero crossing of the input signal in which the nonconduction/conduction transition of the diodes occurs.
- Nevertheless, the use of the high slewrate opamps does not solve this drawback because of its zero transient problem.
- A number of circuits based on various active elements working in VM & CM for realizing full-wave rectification have been reported in the related literature.

Comparison of the proposed rectifier with the previously published ones

VM full-wave rectifier	High input impedance	Low output impedance	Number of active elements	Number of resistors	Number of grounded resistors	Power diss (mW)
Ref. [2]	Yes	No	1 CCII+ current mirrors	2	2	NA
Ref. [3]	Yes	No	2 CCII	2	1	NA
Ref [4]	Yes	No	3 CCCII	5	2	NA
Ref. [5]	Yes	No	1 DO- OTA	1	1	NA
Ref. [6]	No	No	2 CCII 3 NMOS	0	0	NA
Ref. [7]	Yes	No	1 DXCCII 3 NMOS	0	0	3.33
Ref. [8]	Yes	Yes	1 CCII 1OA	3	2	NA
Ref. [9]	Yes	Yes	1 CCII 1 UVC	2	2	NA
Ref. [10]a	Yes	No	2 CCII	3	3	NA
Ref. [10]b	Yes	Yes	1 CCII 1 UVC	2	2	NA
Ref. [11]	Yes	No	2 CCII	3	1	NA
Ref. [12]	Yes	No	2 CCII	2	1	NA
Ref. [13]	No	Yes	2 DVCC 1 NMOS 1 VF	3	0	NA
Ref. [14]	No	No	1 CCII-	2	1	9.25
Ref. [15]	Yes	Yes	1 CCII 28 MOS	1	1	5.2
Proposed rectifier	Yes	Yes	2 DVCC+	2	2	0.93

Circuit Description

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_{Z+} \end{bmatrix} \quad (1)$$

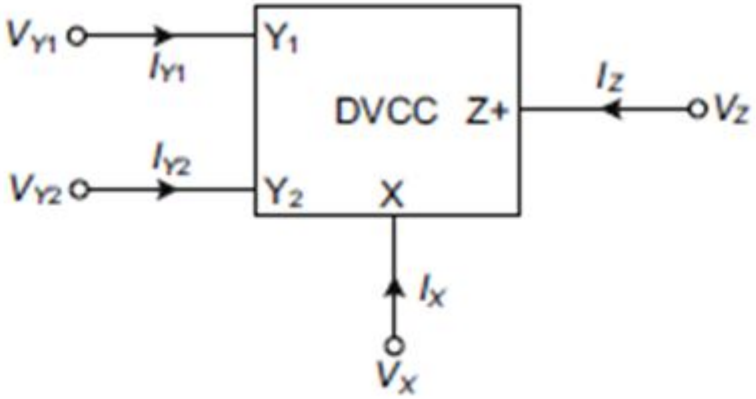


Fig. 1 Electrical symbol of the DVCC+

Circuit description (Cont’d)

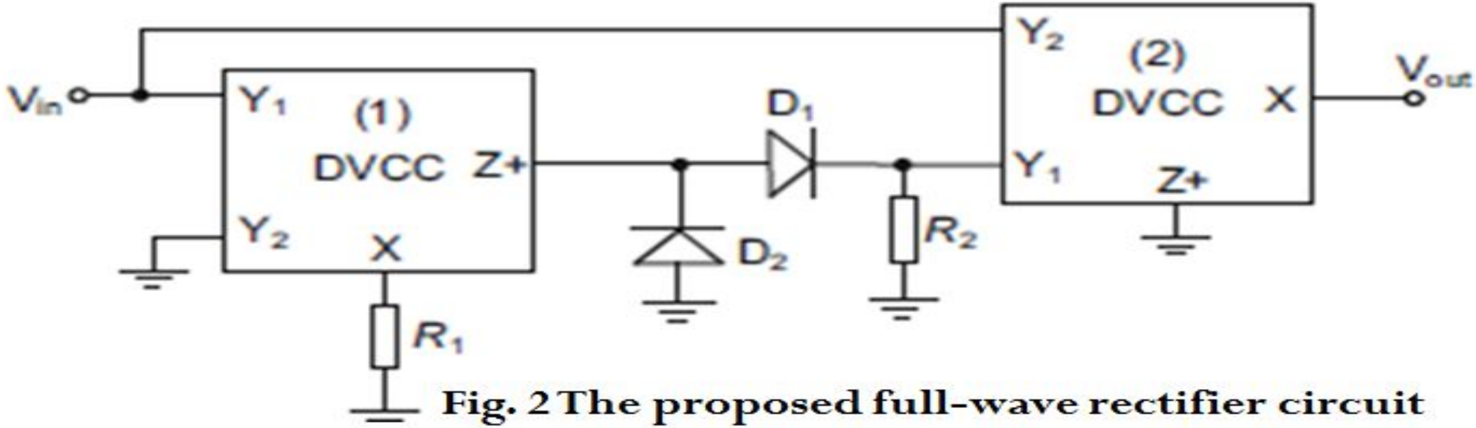


Fig. 2 The proposed full-wave rectifier circuit

$$V_{out} = \left(\frac{R_2}{R_1} - 1\right) V_{in} \qquad (2)$$

If $R_2 = 2R_1$ is chosen in (2), we get

$$V_{out} = V_{in} \qquad (3)$$

$$V_{out} = -V_{in} \qquad (4)$$

Thus, for a full-wave input signal, we get

$$V_{out} = |V_{in}| \qquad (5)$$

Simulation Results

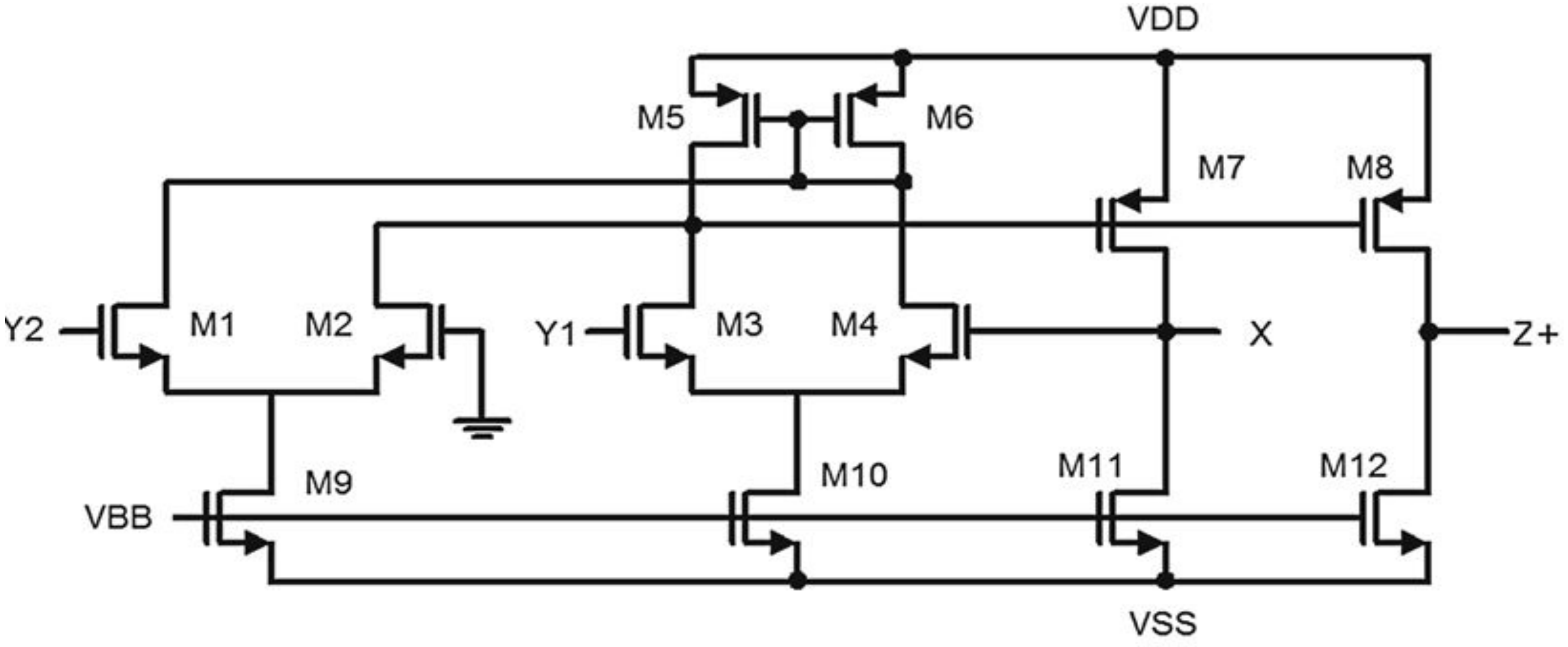
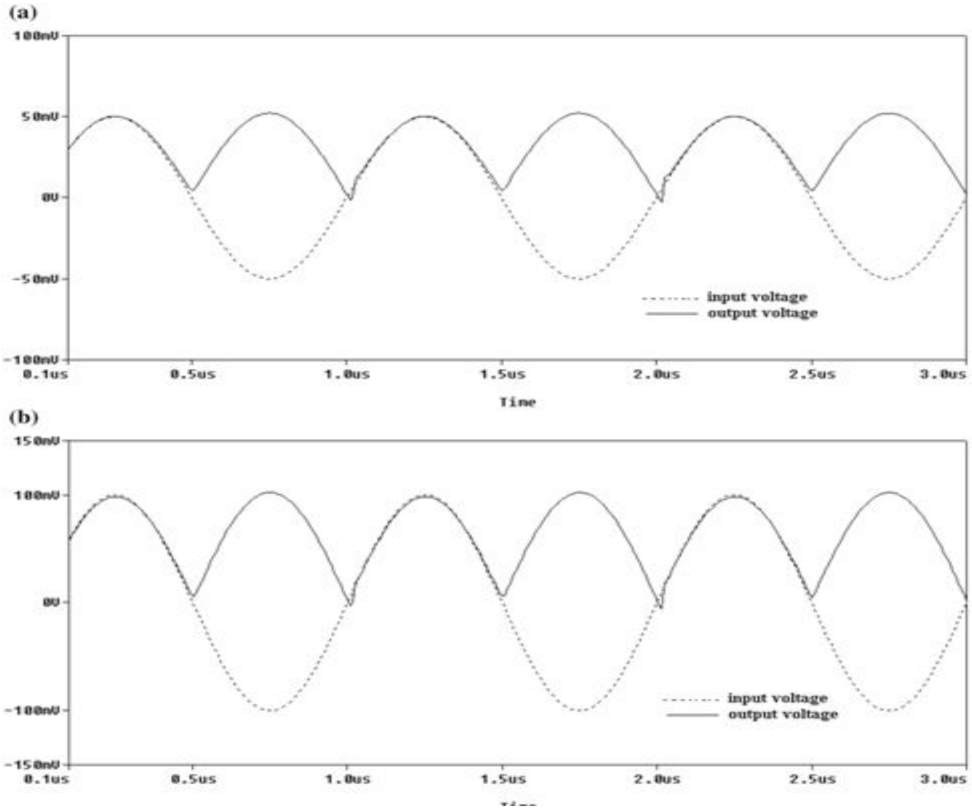


Fig. 4 The CMOS implementation of the DVCC+

Simulation results (Cont'd)



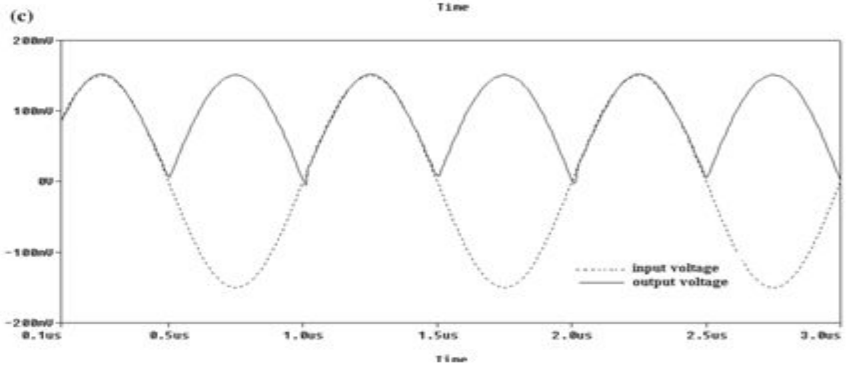


Fig. 10 Simulated transient response at $f = 1$ MHz for Vp = a) 50 mV, b) 100 mV and c) 150 mV

Simulation results (Cont'd)

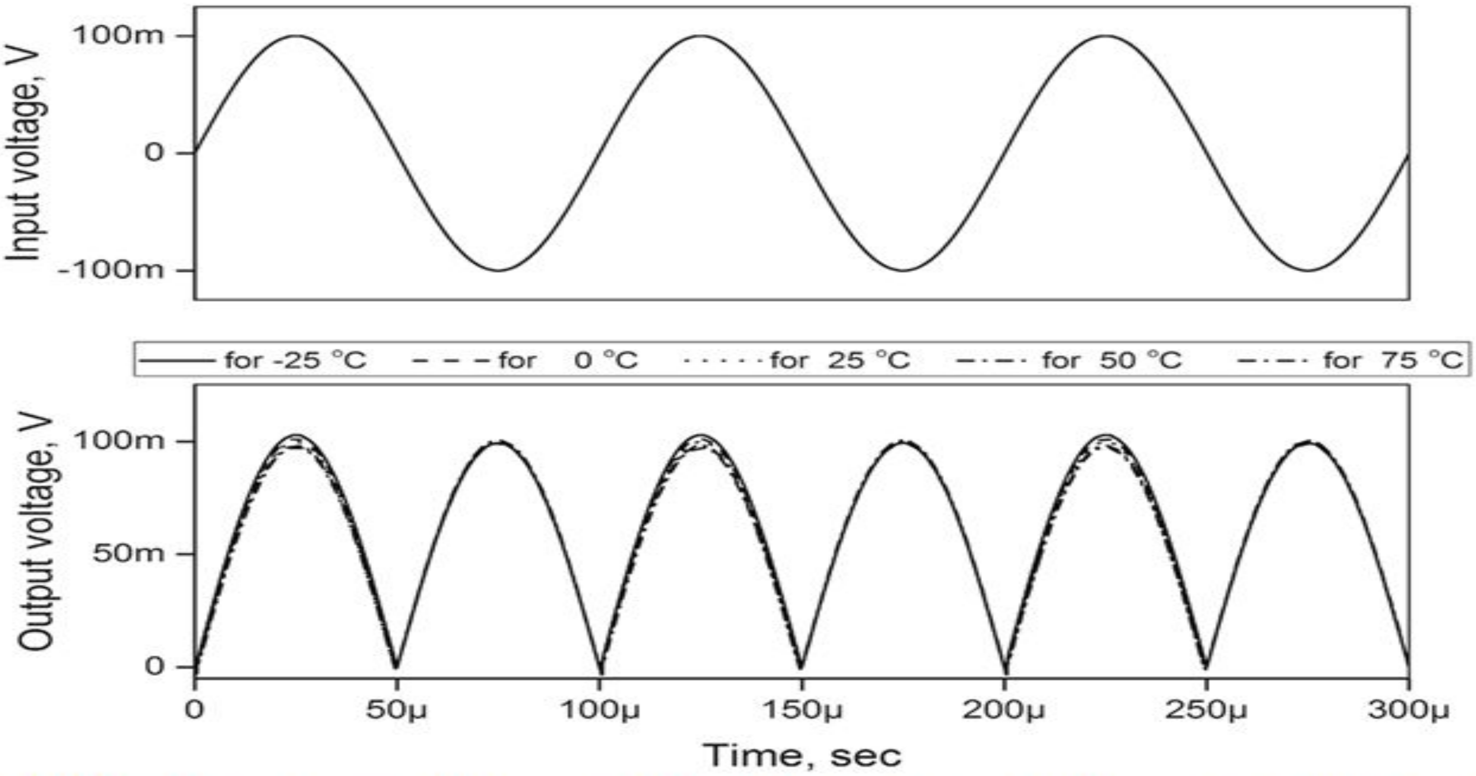


Fig. 13 Transient temperature analysis of the proposed full-wave rectifier circuit

Simulation results (Cont’d)

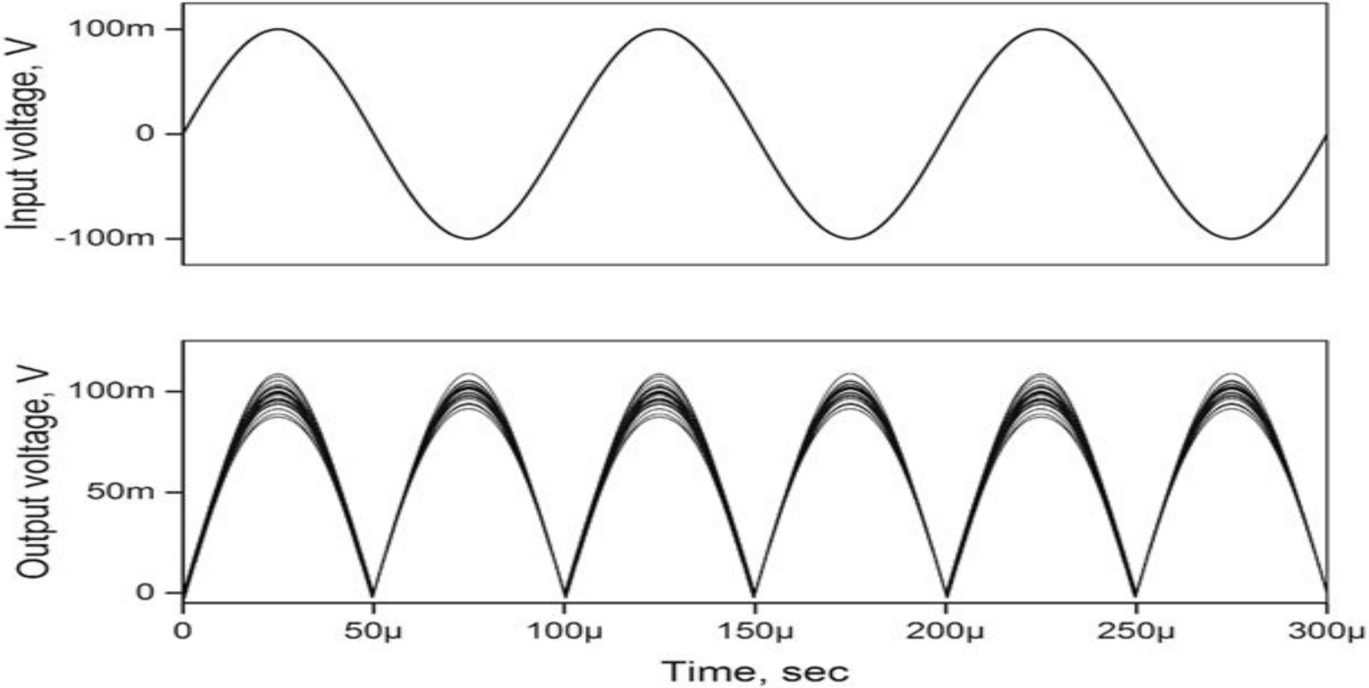


Fig. 14 Transient Monte Carlo analysis of the proposed full-wave rectifier structure

Conclusion

—A new VM precision full-wave rectifier is proposed.

—It has the following features: high input impedance, low output impedance, the need to employ only two DVCC+s, two grounded resistors, and two diodes.

—To be easily cascaded with other VM circuits.

—The use of only grounded resistors is advantageous in IC circuit implementation and parasitic effect cancellation.

—The SPICE simulations confirm the effective operation of the proposed circuit in a wide frequency range.

—However, the difference between ideal and simulation results mainly stems from nonideal gains and parasitic impedances of the DVCC+s.

—It can be useful in many application fields such as signal processing, conditioning, and instrumentation of low-level signal, and DC converters.

Thank You

Questions?